Claims

What is claimed is:

1. A method for forming a non-volatile memory embedded logic circuit comprising the steps of:

providing a semiconductor substrate;

forming an isolation region on said semiconductor substrate to define a first active area, a second active area, and a third active area;

forming a first oxide layer on said first, second, and third active areas simultaneously;

etching said first oxide layer in said first and second active areas to expose said substrate underneath;

forming a second oxide layer in said first active area simultaneously with said and second active area, thereby providing a tunnel oxide layer in said first active area, a low voltage logic gate oxide layer in said second active area, and a high voltage logic gate oxide layer in said third active area; and

forming a floating gate on top of said oxide layers.

2. The method of claim 1, wherein said isolation region is formed by a shallow trench isolation method.

3. The method of claim 1, wherein said isolation region is formed by a local oxidation of silicon method.

4. The method of claim 1, wherein said oxide layers are formed by thermal oxidation.

5. The method of claim 2, wherein said oxide layers are formed by chemical vapor deposition.

6. The method of claim 2, wherein said oxide layers are formed by atomic layer deposition.

7. The method of claim 1, wherein said first oxide layer is approximately 250 Å thick.

8. The method of claim 1, wherein said second oxide layer is approximately 70 Å thick.

9. The method of claim 1, wherein said floating gate layer is a doped polysilicon layer.

10. The non-volatile memory embedded logic circuit of claim 1, wherein said first oxide layer is formed in one processing step.

11. The non-volatile memory embedded logic circuit of claim 1, wherein said second oxide layer is formed in one processing step.

12. A method for forming a non-volatile memory embedded logic circuit comprising the steps of:

providing a semiconductor substrate;

forming an isolation region on said semiconductor substrate to define a first active area and a second active area;

forming a first oxide layer on said first and second active areas simultaneously;

etching said first oxide layer in said first active area to expose said substrate underneath;

forming a second oxide layer in said first active area, thereby providing a tunnel oxide layer in said first active area, and a high voltage logic gate oxide layer in said second active area; and

forming a floating gate layer on top of said oxide layers.

13. The method of claim 10, wherein said oxide layers are formed by thermal oxidation.

14. The method of claim 10, wherein said second oxide layer is approximately 70 Å thick.

15. The method of claim 10, wherein said conductive layer is a doped polysilicon layer.

16. A non-volatile memory embedded logic circuit comprising:

a first active area, a second active area, and a third active area;

a first oxide layer on top of said third active area functioning as a gate oxide for a high voltage logic gate;

a second oxide layer that is thinner than said first oxide layer on top of said first and second active areas, whereby said second oxide layer on top of said first active area functions as a tunnel oxide while said

second oxide layer on top of said second active area functions as a gate oxide for a low voltage logic gate; and

a floating gate layer overlying said first and second oxide layers.

17. The circuit of claim 16, wherein said first oxide layer is approximately 250 Å thick.

18. The non-volatile memory embedded logic circuit of claim 16, wherein said second oxide layer is approximately 70 Å thick.

19. The non-volatile memory embedded logic circuit of claim 16, wherein said floating gate layer is a doped polysilicon layer.

20. The non-volatile memory embedded logic circuit of claim 16, wherein said first oxide layer is formed in one processing step.

21. The non-volatile memory embedded logic circuit of claim 16, wherein said second oxide layer is formed in one processing step.

22. A non-volatile memory embedded logic circuit comprising:

a first active area and a second active area;

a first oxide layer on top of said second active area functioning as a gate oxide for a high voltage logic gate;

a second oxide layer that is thinner than said first oxide layer on top of said first active area, whereby said second oxide layer on top of said first active area functions as a tunnel oxide; and

a floating gate layer overlying said first and second oxide layers.

23. The circuit of claim 22, wherein said first oxide layer is approximately 250 Å thick.

24. The non-volatile memory embedded logic circuit of claim 22, wherein said second oxide layer is approximately 70 Å thick.